providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film so that a crystal growth proceeds in a crystal growth direction parallel to the insulating surface from the first metal element added region and the second metal element added region thereby to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film;

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island using only the first crystalline portion while the second crystalline portion is not used to form the crystalline semiconductor island,

wherein carriers move in the crystalline semiconductor island in a carrier moving direction identical with the crystal growth direction,

wherein the second metal element added region is located apart from the crystalline semiconductor island by a distance,

wherein the first metal element added region has a length extending longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

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7. (Amended) A method according to claim 6, wherein lengths of the first metal element added region and the second element added region are set to 50% or more of a crystal growth distance.

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9. (Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

selectively providing a metal element being capable of promoting crystallization of the amorphous semiconductor film into at least a first region and a second region of the amorphous semiconductor film to form a first metal element added region and a second metal element added region, respectively;

crystallizing the amorphous semiconductor film so that a crystal growths proceed in parallel to the insulating surface from each of the first metal element added region and the second metal element added region to form a first crystalline semiconductor region and a second crystalline semiconductor region, respectively;

forming at least one active region of the semiconductor device in the first crystalline semiconductor region while the second crystalline semiconductor region is not used to form an active region of the semiconductor device.

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11. (Amended) A method according to claim 9, wherein the metal element is provided by an ion implanting method.

12. (Amended) A method according to claim 9, wherein the metal element is provided by coating a solvent comprising the metal element.

14. (Amended) A method according to claim 9, wherein the amorphous semiconductor film comprises silicon.

18. (Amended) A method according to claim 6, wherein the amorphous semiconductor film comprises silicon.

23. (Amended) A method according to claim 9, further comprising controlling crystal growth state using the second metal element added region.

Please add the following new claims 24-71.

24. (New) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to a selected region of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein the metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region.

25. (New) A method according to claim 24,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

26. (New) A method according to claim 24,

wherein the metal element is provided by an ion implanting method.

27. (New) A method according to claim 24,

wherein the metal element is provided by coating a solvent comprising the metal element.

28. (New) A method according to claim 24,

wherein the amorphous semiconductor film comprises silicon.

29. (New) A method according to claim 24,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

30. (New) A method according to claim 24,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

31. (New) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal growths proceed in a direction parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

32. (New) A method according to claim 31,

wherein lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

33. (New) A method according to claim 31,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

34. (New) A method according to claim 31,

wherein the metal element is provided by an ion implanting method.

35. (New) A method according to claim 31,

wherein the metal element is provided by coating a solvent comprising the metal element.

36. (New) A method according to claim 31,

wherein the amorphous semiconductor film comprises silicon.

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37. (New) A method according to claim 31,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

38. (New) A method according to claim 31,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

39. (New) A method according to claim 31, further comprising controlling crystal growth state using a metal element added region that is not used to form crystalline semiconductor islands.

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40. (New) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal growths proceed in a direction parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the

crystalline semiconductor island in a longitudinal direction of a metal element added region, and

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

41. (New) A method according to claim 40,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

42. (New) A method according to claim 40,

wherein the metal element is provided by an ion implanting method.

43. (New) A method according to claim 40,

wherein the metal element is provided by coating a solvent comprising the metal element.

44. (New) A method according to claim 40,

wherein the amorphous semiconductor film comprises silicon.

45. (New) A method according to claim 40,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

46. (New) A method according to claim 40,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

47. (New) A method according to claim 40,

further comprising controlling crystal growth state using a metal element added region that is not used to form crystalline semiconductor islands.

48. (New) A method of manufacturing an inverter circuit, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to a selected region of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein the metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region.

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49. (New) A method according to claim 48,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

50. (New) A method according to claim 48,

wherein the metal element is provided by an ion implanting method.

51. (New) A method according to claim 48,

wherein the metal element is provided by coating a solvent comprising the metal element.

52. (New) A method according to claim 48,

wherein the amorphous semiconductor film comprises silicon.

53. (New) A method according to claim 48,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

54. (New) A method according to claim 48,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

55. (New) A method of manufacturing an inverter circuit, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal growths proceed in a direction parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

56. (New) A method according to claim 55,

wherein lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

57. (New) A method according to claim 55,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

58. (New) A method according to claim 55,

wherein the metal element is provided by an ion implanting method.

59. (New) A method according to claim 55,

wherein the metal element is provided by coating a solvent comprising the metal element.

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60. (New) A method according to claim 55,

wherein the amorphous semiconductor film comprises silicon.

61. (New) A method according to claim 55,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

62. (New) A method according to claim 55,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

63. (New) A method according to claim 55, further comprising controlling crystal growth state using a metal element added region that is not used to form crystalline semiconductor islands.

64. (New) A method of manufacturing an inverter circuit, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal growths proceed in a direction parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the

crystalline semiconductor island in a longitudinal direction of a metal element added region, and

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

65. (New) A method according to claim 64,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

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66. (New) A method according to claim 64,

wherein the metal element is provided by an ion implanting method.

67. (New) A method according to claim 64,

wherein the metal element is provided by coating a solvent comprising the metal element.

68. (New) A method according to claim 64,

wherein the amorphous semiconductor film comprises silicon.

69. (New) A method according to claim 64,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

70. (New) A method according to claim 64,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

71. (New) A method according to claim 64,

further comprising controlling crystal growth state using a metal element added region that is not used to form crystalline semiconductor islands.